

PALM INTRANET

Day : Monday
 Date: 10/15/2007
 Time: 11:13:04

Inventor Name Search Result

Your Search was:

Last Name = TAI

First Name = HUNG-EN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10249147	Not Issued	30	03/19/2003	METHOD OF MANAGING SEMICONDUCTOR MANUFACTURING CASES	TAI, HUNG-EN
10249148	7079677	150	03/19/2003	AN AUTOMATIC INTELLIGENT YIELD IMPROVING AND PROCESS PARAMETER MULTIVARIATE SYSTEM AND THE ANAYSIS METHOD THEREOF	TAI, HUNG-EN
10249213	6968280	150	03/24/2003	METHOD FOR ANALYZING WAFER TEST PARAMETERS	TAI, HUNG-EN
10249375	6904384	150	04/03/2003	COMPLEX MULTIVARIATE ANALYSIS SYSTEM AND METHOD	TAI, HUNG-EN
10604244	6959252	150	07/03/2003	METHOD FOR ANALYZING IN-LINE QC TEST PARAMETERS	TAI, HUNG-EN
10604685	6828776	150	08/11/2003	METHOD FOR ANALYZING DEFECT INSPECTION PARAMETERS	TAI, HUNG-EN
10604979	6898539	150	08/29/2003	METHOD FOR ANALYZING FINAL TEST PARAMETERS	TAI, HUNG-EN
10708277	7099729	150	02/20/2004	SEMICONDUCTOR PROCESS AND YIELD ANALYSIS INTEGRATED REAL-TIME MANAGEMENT METHOD	TAI, HUNG-EN
10708572	6950783	150	03/11/2004	METHOD AND RELATED SYSTEM FOR SEMICONDUCTOR EQUIPMENT PREVENTION MAINTENANCE MANAGEMENT	TAI, HUNG-EN
10708573	6999897	150	03/11/2004	METHOD AND RELATED SYSTEM FOR SEMICONDUCTOR EQUIPMENT EARLY WARNING MANAGEMENT	TAI, HUNG-EN
10711179	Not Issued	30	08/30/2004	DATA ANALYZING METHOD FOR A FAULT DETECTION AND CLASSIFICATION SYSTEM	TAI, HUNG-EN
10711310	Not	30	09/09/2004	Method of Managing Wafer Defects	TAI, HUNG-EN

	Issued				
11401900	7218981	150	04/12/2006	DISPATCH INTEGRATION SYSTEM AND METHOD BASED ON SEMICONDUCTOR MANUFACTURING	TAI, HUNG-EN

Inventor Search Completed: No Records to Display.

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PALM INTRANETDay : Monday
Date: 10/15/2007
Time: 11:13:46**Inventor Name Search Result**

Your Search was:

Last Name = CHEN

First Name = CHIA-YUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10711310	Not Issued	30	09/09/2004	Method of Managing Wafer Defects	CHEN, CHIA-YUN
10904873	Not Issued	41	12/01/2004	METHOD OF DEFECT INSPECTION	CHEN, CHIA-YUN
11213931	7132354	150	08/30/2005	INSPECTION METHODS FOR A SEMICONDUCTOR DEVICE	CHEN, CHIA-YUN
11892759	Not Issued	17	08/27/2007	Man-made material presenting magnetic response at different frequencies	CHEN, CHIA-YUN
11653458	Not Issued	25	01/16/2007	Lower mold assembly for punching a sheet	CHEN, CHIA-YUNG
11540953	Not Issued	41	10/02/2006	Three-dimensional combining structure for an auxiliary lens set	CHENG, CHIA-YUNG

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name	
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PALM INTRANET

Day : Monday
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Inventor Name Search Result

Your Search was:

Last Name = WANG

First Name = SHENG-JEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09940852	6531776	150	08/29/2001	SEMICONDUCTOR DEVICE HAVING REDUCED INTERCONNECT-LINE PARASITIC CAPACITANCE	WANG, SHENG-JEN
10249103	6807454	150	03/17/2003	METHOD FOR AUTOMATICALLY CONTROLLING DEFECT - SPECIFICATION IN A SEMICONDUCTOR MANUFACTURING PROCESS	WANG, SHENG-JEN
10249147	Not Issued	30	03/19/2003	METHOD OF MANAGING SEMICONDUCTOR MANUFACTURING CASES	WANG, SHENG-JEN
10249148	7079677	150	03/19/2003	AN AUTOMATIC INTELLIGENT YIELD IMPROVING AND PROCESS PARAMETER MULTIVARIATE SYSTEM AND THE ANALYSIS METHOD THEREOF	WANG, SHENG-JEN
10708277	7099729	150	02/20/2004	SEMICONDUCTOR PROCESS AND YIELD ANALYSIS INTEGRATED REAL-TIME MANAGEMENT METHOD	WANG, SHENG-JEN
10708572	6950783	150	03/11/2004	METHOD AND RELATED SYSTEM FOR SEMICONDUCTOR EQUIPMENT PREVENTION MAINTENANCE MANAGEMENT	WANG, SHENG-JEN
10708573	6999897	150	03/11/2004	METHOD AND RELATED SYSTEM FOR SEMICONDUCTOR EQUIPMENT EARLY WARNING MANAGEMENT	WANG, SHENG-JEN
10711310	Not Issued	30	09/09/2004	Method of Managing Wafer Defects	WANG, SHENG-JEN
11228361	7260444	150	09/19/2005	REAL-TIME MANAGEMENT SYSTEMS AND METHODS FOR MANUFACTURING MANAGEMENT AND YIELD RATE ANALYSIS INTEGRATION	WANG, SHENG-JEN

Inventor Search Completed: No Records to Display.

Search Another: Inventor	Last Name	First Name	Search
	WANG	SHENG-JEN	

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2	BRS	0	S3 and server adj integrate with wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	0	S3 and (pre adj treatment or pre-treatment)and server and integrate and wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	0	S3 and server and integrate and wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
5	BRS	25	inspect\$3 and (wafer\$1 or semicondutor\$1 or chip\$1 or substrat\$1 or IC or intergrated adj circuit or PCB or printed adj circuit adj board or PWB or printed adj wiring adj board)and generat\$3 adj defect\$3 and raw adj data	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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7	BRS	2	S12 and (@ad<"20040909" or @rlad<"20040909" or @prad<"20040909" or @ptad<"20040909")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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9	BRS	3	S2 and server and integrat\$3 and wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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11	BRS	0	S3 and server adj integrate and wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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13	BRS	14	S2 and (@ad<"20040909" or @rlad<"20040909" or @prad<"20040909" or @ptad<"20040909")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
14	BRS	0	S3 and server adj integrat\$3 and wafer\$1 adj defect\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
15	BRS	2	"7103210".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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